DEMONSTRATION OF PHOTONICALLY-CONTROLLED GAAS DIGITAL/MMIC FOR RF OPTICAL LINKS

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ABSTRACT

We report design, fabrication, and test of a monolithic GaAs IC implementing a broadband optically-driven digital/analog RF interface. The circuit operates in an asynchronous mode to detect AM digital and RF on a single optical fiber input, control RF level, and transmit the RF to the output.

INTRODUCTION

Lightwave communications for local interconnections within an RF system will yield savings in weight and simplified physical structure by replacing copper cabling and waveguide with optical fiber, provided the optical communications subsystem is optimized for the special needs of the RF system. Present-day RF systems require broadband, low noise analog interconnections with tight control of effective line length (time delay/phase shift) as well as megabit/s digital links. The ubiquity of GaAs in RF systems and its good properties as a photodetector suggest use of a 0.85 μm wavelength, which can be directly detected on a GaAs IC. The economics of local interconnects in RF systems–hundreds or thousands of parallel short-haul links–are quite different from those of long-haul multiple-subscriber telecommunications. The on-chip integration possibility offered by the choice of a GaAs-compatible wavelength is key.

To explore some of the capabilities of this technology, we have designed, fabricated, and tested a photonic digital/RF monolithic interface IC suitable for use in a phased array, towed RF decoy, missile seeker, or other RF system needing broadband, stable communication links implemented in an integrated, low-cost, foundry-compatible technology. The GaAs monolithic IC includes an on-chip MSM (metal-semiconductor-metal) photodetector, low-frequency signal-conditioning circuitry, RF transimpedance amplification, a low-noise amplifier, a 3-bit digitally-controlled attenuator, and an error-detecting digital interface driving a serial-to-parallel converter which then controls the attenuator. We have demonstrated transmission of the digital commands and cw RF (as AM on an optical carrier at 0.85 μm wavelength) over a single fiber proximity-coupled to the on-chip photodetector and subsequent control of the output RF level in accordance with the simultaneously-transmitted digital serial commands. Inputs to the chip, in addition to the lightwave, were power and ground. Combining in a monolithic format optical detection, digital circuitry, and analog microwave circuitry, this is the first IC of this type ever reported.

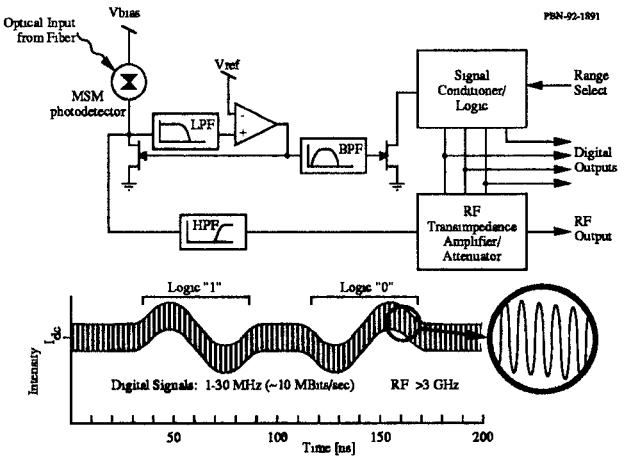

Figure 1. Block diagram and schematic signals used for the MOE1 demonstration IC.

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Design of the IC

Figure 1 shows a block diagram of this Microwave OptoElectronic IC (MOE1). The planar structure of the MSM photodetector used on-chip is nearly ideal for RF/digital signal detection Under time-varying illumination it acts as an almost-ideal current source with high detection efficiency (0.41 A/W) and low capacitance (~50 fF). Photocurrent consists of three components, as shown in the lower half of the figure. There is a dc part, 1.7 mA in amplitude in the test setup we used. Superimposed on this is an ac signal, with a modulation index of 0.09, comprising cw RF (3 GHz in our measurements) and "low-frequency" (LF) digital signals in the 1-30 MHz band. In the amplifier shown the dc and LF signals are fed back to maintain the voltage at the drain of the main current-sink FET constant against variations up to about 50 MHz. RF is outside the band of this feedback circuit and therefore appears across the drain impedance of this FET. It is amplified by the RF chain and then fed to a 3-bit digital attenuator. Additional circuitry is included on this first IC for testability.

The digital signaling, as shown in the figure, uses a zero-dc-power scheme with a high-low sequence for a logic 1 and a low-high for logic 0. This waveform allows self-clocking, detection of noise pulses (high with no low or vice versa), and clean separation of the frequency bands. Received digital bits are shifted into an on-chip shift register. The first bit must be a 1. When it reaches the fourth register bit, on-chip circuitry generates a "LOAD" pulse which transfers bits 2, 3, and 4 from the shift register into the control register connected to the RF attenuator. One more received bit then shifts the leading 1 bit into the fifth register bit, which engenders a "CLEAR" signal which zeroes the shift register (without affecting the control register) in preparation for the next command word. The entire process is asynchronous and self-clocked.

The RF chain starts with a transimpedance amplifier (XZAMP) to interface the low-power high-impedance RF voltage available at the drain of the main current-sink FET to the following RF circuitry, which is designed as 50-Ω blocks. The XZAMP is designed for a nominal gain of 40 dBΩ, i.e. a transimpedance of 100 Ω. The XZAMP is followed by a LNA whose gain cancels the insertion loss of the final RF circuit block, a digitally-controlled 3-bit attenuator.

The IC was designed to be fabricated on Raytheon Research Division's Enhancement/-Depletion prototype line. This process is the basis for a foundry process now in production at Raytheon. The process uses 0.5 μm gate length and yields Enhancement/Depletion (E/D) MESFETs with maximum f_T of 30 GHz and f_{max} above 60 GHz.

The EFET and DFET channels are formed by selective ion implantation of Si and Be. The nominal threshold voltages for the EFETs and DFETs are +0.1 V and -0.5 V, respectively. The source and drain ohmic contacts are formed on N^+ regions of the FET, with a sheet resistance of 200 Ω/square. Gate material is Ti/Pt/Au and the recess depth is ≈400 Å. The process also features GaAs implanted resistors (which use unrecessed EFET Channel implant) with a sheet resistance of 750 Ω/square; low temperature coefficient (<200 ppm/C) 6 Ω/square TaN resistors; 300 pF/mm^2 MIM capacitors with 2000 Å SiN dielectric; air bridges; and low loss inductors and transmission lines. The standard deviation of the threshold voltage is 22 mV across a given 3" wafer. The maximum EFET transconductance is 275 mS/mm; the breakdown voltage is ≥9 V. Except for the gate, which is E-beam written, all lithography steps are done with an I-line stepper. The process includes two levels of interconnect Ti/Pt/Au metal with sheet resistances of 100 and 30 mΩ/square respectively, the top level being used for 3 μm-thick transmission lines as well as digital interconnect.

The process has been used to make ICs with both digital and MMIC circuitry on a single chip and has been used on a number of demonstration projects. No extra masking layers were needed for the MSM detector fingers, which were written at the same time as the gates, and which are formed of 0.5 μm line-and-space interdigitated electrodes on undoped GaAs.

Results

A comparison between the modeled and measured performance of MOE1 is shown in Figure 2. For this test the RF chain was driven through an on-chip 1.8 kΩ resistor to simulate the effects of a high-impedance source (the MSM); this results in a return loss of nominally 0 dB as shown.

Figure 3 shows the measured output RF stepping through seven controlled states as digital words commanding them are shifted in. Note

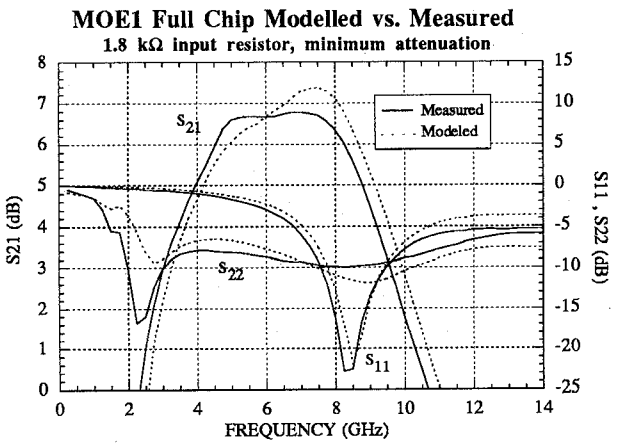

Figure 2. Electrical performance of the MOE1 IC. A photodetector-like input is simulated by using an on-chip 1.8 kΩ series input resistor.

that the RF amplitude is unaffected by the digital shifting (it takes five bits transmitted to change from one state to the next).

The overall RF signal level at the output of the IC was -41 dBm into 50 Ω with the optical input just described having approximately 160 μW of RF modulation.

This project demonstrates the viability of such ICs and brings the idea of photonic RF interconnects to fruition for the first time. The importance of a foundry-qualified photonic-link capability in assuring timely insertion of photonics into a wide variety of RF subsystems is a key factor in the choice of 0.85 μm wavelength for this demonstration.

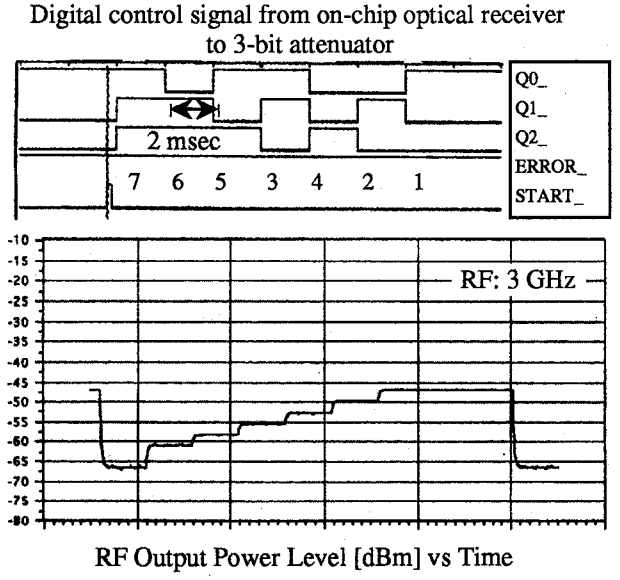

Figure 3. Operation of the MOE1 IC. The output is from a spectrum analyzer set at a fixed frequency, 3 GHz. A 5-bit digital word is shifted into the IC over its optical fiber to change the state of the on-chip attenuator for each of the sequential output level changes shown.